What is claimed is:

1. An automatic design system for designing wirings on circuit elements comprising:

an input device configured to receive circuit information on logic circuits scheduled to be layouted on a large-scale integrated circuit;

a glitch searching unit configured to search a glitch-occurring circuit element in the logic circuits to which a glitch occurs;

a skew calculator configured to calculate a skew of a clock signal to be fed to the glitch-occurring circuit element;

a circuit information analyzer configured to define the calculated skew as a first target skew and determine whether the glitch can be reduced by setting the first target skew to F/Fs; and

a first target skew setting unit configured to set the first target skew to the F/Fs when the circuit information analyzer determines that the glitch can be reduced.

2. The automatic design system of claim 1, further comprising:

a first latch insertion unit configured to insert a first latch in a signal propagation path starting form an output side of a glitch-occurring circuit output side of the circuit element when the circuit information analyzer determines that the glitch cannot be reduced.

3. The automatic design system of claim 1, further comprising:

a clock wiring processing unit configured to perform clock wiring in the logic circuits subject to any setting of the first target skew;

a timing verification unit configured to verify whether a timing constraint to allow the logic circuits to operate normally is satisfied after the clock wiring; and

a second target skew setting unit configured to set a second target skew in the logic circuits to satisfy the timing constraint when the timing verification unit verifies that the timing constraint is not satisfied.

4. The automatic design system of claim 2, further comprising:

a clock wiring processing unit configured to perform clock wiring in the logic circuits subject to any setting of the first target skew and insert the first latch;

a timing verification unit configured to verify whether a timing constraint to allow the logic circuits to operate normally is satisfied after the clock wiring; and

a second latch insertion unit configured to insert a second latch in the logic circuits to satisfy the timing constraint when the timing verification unit verifies that the timing constraint is not satisfied.

5. The automatic design system of claim 2, further comprising:

a glitch-attributed power dissipation estimation unit configured to estimate glitch-attributed power dissipation in the logic circuits before and after setting any one of the first target skew and a second target skew;

an overall power dissipation estimation unit configured to estimate overall power dissipation of the clock wiring and the circuit element before and after setting any one of the first target skew and the second target skew; and

a circuit power dissipation comparator configured to compare an increase and decrease in the glitch-attributed power dissipation and an increase and decrease in the overall power dissipation.

6. An automatic design system comprising:

an input device configured to receive circuit information on logic circuits designed by a gated clock design and being scheduled to be layouted on a large-scale integrated circuit;

a first timing verification unit configured to verify whether a timing constraint for allowing the logic circuit to operate normally is satisfied;

a first clock wiring processing unit configured to perform clock wiring on the logic circuits;

a second timing verification unit configured to verify whether the logic circuits after the clock wiring satisfies the timing constraint;

a slack value calculator configured to calculate the maximum slack value out of critical paths which do not satisfy the timing constraint when the second timing verification unit verifies that the timing constraint is not satisfied; and

a target skew setting unit configured to set a target skew so as to render the slack value positive.

7. The automatic design system of claim 6, further comprising:

a second clock wiring processing unit configured to perform clock wiring after setting the target skew so as to satisfy the target skew.

8. A computer implemented wiring method for designing wirings on circuit elements comprising:

supplying circuit information on logic circuits scheduled to be layouted on a large-scale integrated circuit;

searching a glitch-occurring circuit element in the logic circuits to which a glitch occurs;

calculating a skew of a clock signal to be fed to the glitch-occurring circuit elements;

analyzing whether the glitch can be reduced by setting the calculated skew as a first target skew to F/Fs; and

setting the first target skew to the F/Fs when a determination is made that the glitch can be reduced.

9. The method of claim 8, further comprising:

inserting a first latch in a signal propagation path starting from an output side of the glitch-occurring circuit when it is determined that the glitch cannot be reduced.

10. The method of claim 8, further comprising:

performing clock wiring in the logic circuits subject to any setting of the first target skew;

verifying whether a timing constraint to allow the logic circuits to operate normally is satisfied after the clock wiring; and

setting a second target skew in the logic circuits to satisfy the timing constraint when a verification determines that the timing constraint is not satisfied.

11. The method of claim 9, further comprising:

performing clock wiring in the logic circuits subject to any setting of the first target skew and insert the first latch;

verifying whether a timing constraint to allow the logic circuits to operate normally is satisfied after the clock wiring; and

insert a second latch in the logic circuits to satisfy the timing constraint when a verification determines that the timing constraint is not satisfied.

12. The method of claim 9, further comprising:

estimating glitch-attributed power dissipation in the logic circuits before and after setting the target skew;

estimating overall power dissipation of wiring and the circuit element before and after setting the target skew; and

comparing an increase and decrease in the glitch-attributed power dissipation and an increase and decrease in the overall power dissipation.

13. A computer implemented wiring method comprising:

supplying circuit information on logic circuits designed by a gated clock design and being scheduled to be layouted on a large scale integrated circuit;

verifying whether a timing constraint for allowing the logic circuit to operate normally is satisfied;

performing clock wiring on the logic circuits;

verifying whether the logic circuits after the clock wiring satisfies the timing constraint;

calculating the maximum slack value out of critical paths which do not satisfy the timing constraint when the timing constraint is not satisfied; and

setting a target skew so as to render the slack value positive.

14. The method of claim 13, further comprising:

performing clock wiring after setting the target skew so as to satisfy the target skew.